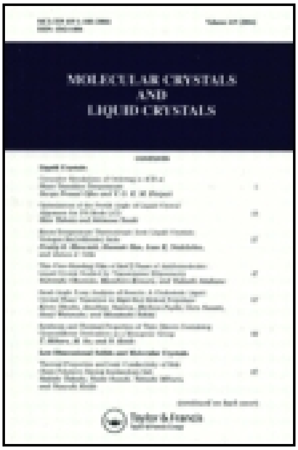

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Fabrication of Vertical Organic Field Effect Transistor at the Edge of Patterned Photoresist

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The organic field effect transistors having a very short channel length of 0.3 μm was fabricated by means of "self-alignment method." This device has a vertical channel between the electrodes upon and under a photoresist film and the channel length can be controlled by the thickness of the photoresist. The current modulation by gate voltage was successfully observed in this vertical structure. This device showed large current modulation reaching 100 μA by relative low source-drain voltage up to 5 V, which was attributed to the short channel length.

Keywords: organic field effect transistor; short channel length; vertical structure

INTRODUCTION

Organic field effect transistors (OFET) usually have a planar structure where the source and drain electrode is separated using some patterning techniques, such as shadow mask or lithography. The channel length corresponding to the gap between the source and drain electrode affects the saturated drain current and cut-off frequency, even though the same organic material is used for the channel layer. Therefore, shorter channel length is aspired to achieve higher current operation and higher frequency response. However, it is difficult to make it shorter less than an order of microns as long as planar structures are adopted, in particular, in the case of top-contact structures requiring a shadow mask deposition.

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There have been many reports attempting to shorten the channel length [1,2]. One of the ways to drastically shorten it is "vertical structure," where the channel carriers flow across the thin film in vertical direction to the substrate. Static Induced Transistor [3], Top and Bottom Contact Transistors [4], and Charge Injection Controlled transistors [5] are known as this type. Recently, such a vertical channel FET having a channel length of 2.4 μm was reported using an edge of the photoresist film [6].

In this study, we fabricated this edge-type OFET, but having much shorter channel length of 0.3 μm by means of "self-alignment method" to achieve a steep edge and precise positioning of the upper electrode. These devices have a vertical channel between the electrodes upon and under the photoresist, therefore, the channel length can be controlled by the thickness of photoresist film.

EXPERIMENT

The device structure and fabrication process are shown in Figure 1. The device has the top-gate and top-contact structure with the vertical channel. At first, an ITO/glass substrate was baked by a hot plate at 150°C for 30 min. After the primer coating, the positive-type photoresist (OFPR-800, supplied from Tokyo Ohka Kogyo Co., Ltd.) diluted by acetone was spin-coated. Cr (2 nm) and Au (30 nm) were deposited

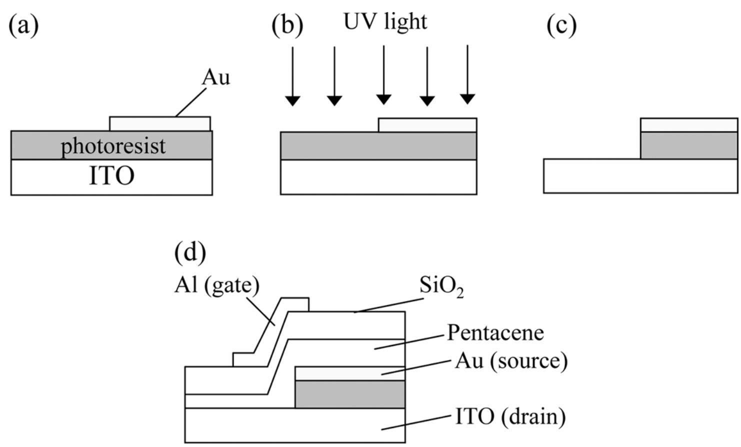

FIGURE 1 Schematic illustration of the fabrication process of 'self-alignment method' and the final device structure. (a) spin-coating of photoresist and Au deposition, (b) UV exposure through the Au film, (c) development, (d) the final structure of a vertical transistor.

with a shadow mask as an upper electrode. After baking at 90°C for 20 min, UV-light was exposed for 5 s through the deposited Au electrode used as a shadow mask. The exposed photoresist was rinsed by the developer for 30 s. Thus, the vertical channel, where the upper Au electrode and bottom ITO electrode were separated by photoresist, was obtained.

Next, the channel layer of pentacene was deposited with thickness of 75 nm and deposition rate of 0.1 nm/s. The base pressure was 1.0×10^{-5} torr. Pentacene supplied from Aldrich Co. Ltd. was purified twice by train sublimation technique. The gate-insulating layer of 150 nm-thick SiO_2 layer was prepared by depositing SiO under oxygen pressure of 1×10^{-4} torr. Finally, the Al gate electrode of 30 nm-thick was deposited on the top of the films at deposition rate 0.4 nm/s.

The structure of the vertical channel was evaluated by scanning electron microscopy (SEM). The current characteristics were measured using a semiconductor parameter analyzer unit (Agilent Technologies, Model 4155). All the measurements were performed at room-temperature and under vacuum condition of 1.0×10^{-3} torr.

RESULTS AND DISCUSSION

The vertical structures composed of source and drain electrodes separated by a photoresist film were evaluated using SEM. Figure 2(a) shows its cross-sectional image before deposition of an organic layer. The photoresist film was sharply removed at the edge of deposited upper electrode. When the exposure time and developing time were optimized, electric shortage between ITO and Au electrode was not

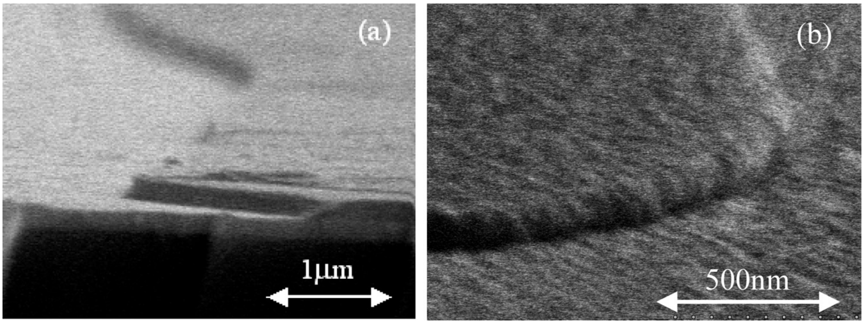

FIGURE 2 Cross-sectional SEM images of the vertical strucure composed of ITO/photoresist/Au. (a) before deposition of an organic layer, (b) after deposition of pentacene of 75 nm-thick.

observed. Figure 2(b) shows the vertical structure after depositing pentacene of 75 nm. The crystalline grains of pentacene covered the sharp drop in level at the edge. Thus, we obtained vertically gapped electrodes having a channel length of 0.3 μm, which corresponds to the thickness of photoresist film. This self-alignment method can achieve very short channel without complicated techniques like electron beam or carefully mask alignment.

Figure 3 shows the output characteristics under different gate voltages from 0 V to 8 V. The current modulation by gate voltage was observed in this vertical structure. In spite of low voltage around 5 V, the modulated current reached 100 μA (channel width = 5 mm). These results are attributed to the advantage of the vertical structure having very short channel length. On the other hand, ON/OFF ratio remained lower value of ~50.

The shapes of the drain current – drain voltage curves were more or less different from those of conventional FETs. The $I_D - V_D$ curves can be divided into three regions. In a lower drain voltage region less than 5 V, large current modulation was observed. Then, the modulated current slightly decreased in the drain voltage around 7 V. Finally, the drain current rose up sharply with increasing drain voltage from 8 V to 10 V. The decrease of current in the second region seems to be due to current drift, because this device has a slight hysteresis. The current divergence in the third region seems to be attributed to punch-through effect, where the carrier charges are injected from the electrode and flow through the channel without gate voltage.

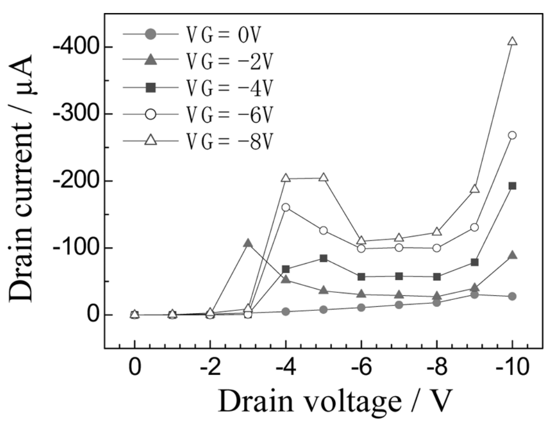

FIGURE 3 Current modulation of vertical organic FET with pentacene (75 nm), SiO_2 (150 nm) and Al gate electrode (30 nm).

On the other hand, the dependence of the divergence current component on the gate voltage suggests another effect because the punch-through current is not dependent on the gate voltage. The detail is not clear, but that behavior may be explained by the injected current modulated by the vertical electric field of the gate voltage.

If we assume that the second region of the $I_D - V_D$ curves shows the saturated current, and if we can evaluate the mobility using the same method as the case of conventional FET, then the field effect mobility can be estimated to be $8.08 \times 10^{-3}\,cm^2/Vs$. In this case, the channel length was assumed to $0.3\,\mu m$ that is the thickness of photoresist. On the other hand, the normal "lateral" FET with the top gate and bottom contact structure using the same pentacene and SiO_2 layers indicated low mobility of an order of $10^{-4}\,cm^2/Vs$. This means that the interface between pentacene and deposited SiO_2 is not ideal in our condition. Nevertheless, the vertical transistor showed higher performance. This result suggests not only an advantage of the short channel length, but also that the modulation mechanism is slightly different from the conventional FET. That is to say, the interface between the insulator and the semiconductor may be not crucial in this device structure.

The estimated field effect mobility is relatively lower than the top data of a pentacene film. There are three possibilities to explain this result. One is the same reason why lower mobility is observed in the bottom contact device of FETs, compared to the top contact device. It is generally known that organic FETs with bottom contact structure have disadvantages because the injection area of the source electrode is very narrow and the carrier injection is prevented by the large contact resistance. The second is structural disorder around the electrodes. The film formation by vacuum deposition is strongly dependent on the material and structure of the substrate. We confirmed that the deposited pentacene film on the photoresist layer had the same crystallinity as that on the silicon substrate by X-ray diffraction measurements. However, the structure of the electrode edge is more complicated as shown in Figure 2.

The third explanation results from the vertical structure. We used pentacene, which is well known as good material for planar FET. However, it is not necessary suitable for the vertical structure, because the direction of carrier flow is different from the conventional lateral FETs. The high performance of pentacene is attributed to its molecular arrangement, where the molecular stands on the substrate and forms high mobility π-stacking between the source and drain electrodes. Therefore, there may exist more suitable materials than pentacene for the vertical structure, which has been thought to be useless in conventional FETs.

CONCLUSION

In conclusion, we fabricated a vertical channel FET having a very short channel of 0.3 μm. The self-alignment method enabled us to make this structure more simply. The device showed large current modulation with relatively low source-drain voltage, which would be attributed to the short channel length.

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